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Process Issues in the Development of a Ferroelectric Capacitor/CMOS Test Chip

by Bernard J. Rod

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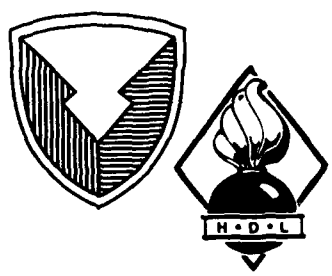

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Bernard J. Rod

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Harry Diamond Laboratories
2800 Powder Mill Road
Adelphi, MD 20783-1197

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13. ABSTRACT *(Maximum 200 words)*

Processing details are discussed in the development of a procedure to fabricate lead-zirconate-titanate (PZT) ferroelectric capacitors on a CMOS test chip for purposes of electrical and radiation characterization studies. During the course of this work, several problems were encountered in the deposition and photoengraving of the platinum electrodes that form the conducting plates of the capacitor. Both dry and wet etching techniques were employed in an effort to define the top platinum electrodes. Solutions are discussed for those problems solved during this initial development phase.

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1. Introduction

During the last few years, considerable interest has been rekindled in the application of ferroelectric materials to the fabrication of nonvolatile random-access memories (RAM's) that employ a ferroelectric capacitor as the basic memory element [1–3]. Ferroelectric memories would be expected to be superior to memories based on standard technologies not only because of their nonvolatility, but also because the ferroelectric capacitor memory element itself is inherently radiation hard. Both these advantages would be of considerable importance to advanced Army ground and space-based electronics systems. This report discusses the work done to develop a ferroelectric memory element test chip compatible with complementary metal-oxide semiconductor (CMOS) integrated circuit processing; the resulting chip would be used in electrical and radiation characterization studies for nonvolatile memory development. The first phase of this effort, reported herein, has been concerned with determining a CMOS-compatible process to define the basic ferroelectric capacitor structure, as shown in figure 1. Etching of the ferroelectric, the deposition and etching of electrically compatible top and bottom electrodes, and the choice of suitable compatible etching techniques were the technical areas that received the major share of attention during this initial development phase.

Any number of different approaches can be taken to fabricate a working ferroelectric capacitor as an independent device in itself. However, when the capacitor is to be incorporated onto an existing CMOS integrated circuit wafer, a number of constraints are necessarily placed on its fabrication. The effects of high temperatures after integrated circuit processing, exposure to potentially contaminating substances, and the removal or chemical attacking of the underlying circuitry by the process chemicals are all concerns that must be adequately addressed in producing a CMOS-compatible ferroelectric memory element. Thus, the compatibility of the ferroelectric capacitor process with the CMOS circuitry is the critical issue.

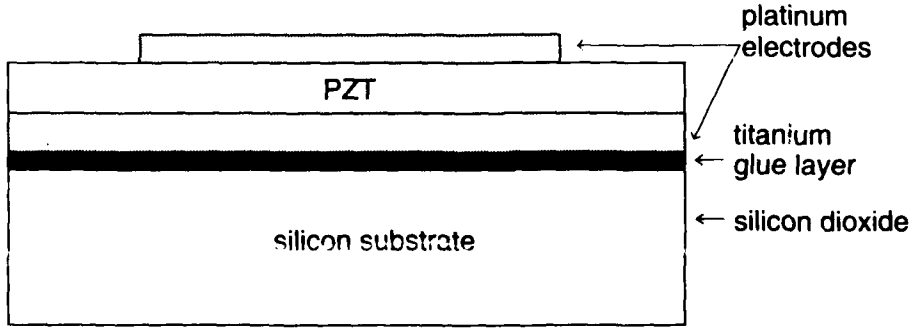


Figure 1. Ferroelectric capacitor cross section.

All the work discussed herein is based on processing of lead zirconate titanate (PZT) ferroelectric films deposited by the sol-gel process [4–5]. Figure 2 shows a typical sol-gel deposition process used for all films studied here. The film thicknesses ranged from approximately 1700 to 6000 Å. For this initial effort, platinum-sputtered silicon substrates with these films already applied were obtained from outside sources.

2. Process Development

The first process investigation was concerned with the etching of the sol-gel deposited ferroelectric films in order to define the capacitor body. Using a recipe obtained from outside sources, we did initial etching experiments at room temperature with a mixture of buffered hydrofluoric acid (seven parts ammonium fluoride solution to one part 48-percent hydrofluoric acid) and hydrochloric acid, followed by a brief dip in dilute nitric acid to remove the lead oxide film that remained after the bulk of the ferroelectric film had been removed. Standard integrated-circuit photoresist masking techniques using KTI 825 30-centistokes resist, spun on to a thickness of 1.2 μm, were used to define the PZT patterns. However, the ferroelectric films etched very slowly, resulting in an unacceptable amount of undercut-

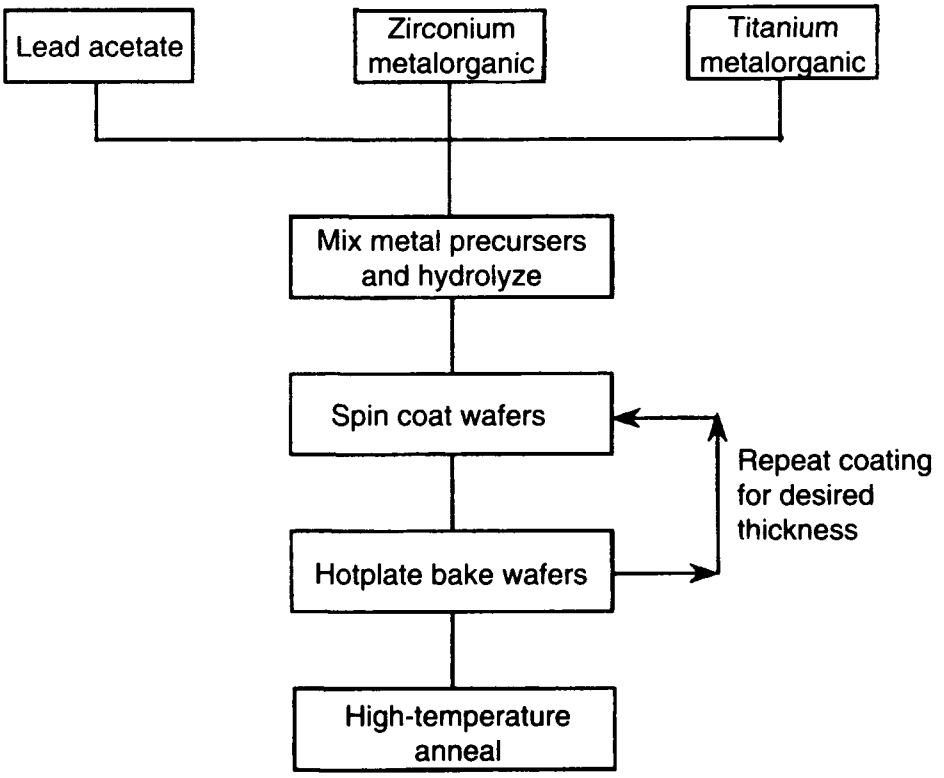


Figure 2. Typical sol-gel process flow.

ting of the photoresist, and the lead residue remaining was considerable. Subsequent experimentation showed that a more uniform and controlled etching procedure could be obtained using the buffered hydrofluoric acid by itself, followed by a brief dip in 5-percent nitric acid to remove the remaining lead-rich residue. Etch rates of approximately 1100 Å per minute at room temperature were obtained. With this technique, well-defined PZT patterns could be obtained, as shown in figure 3.

Also addressed in this initial effort were the critical steps of depositing and defining the platinum top and bottom electrodes of the ferroelectric capacitor. For the top electrode, the platinum is used by itself. For the bottom electrode, a thin glue layer of titanium or chrome is required to be sputtered between the silicon dioxide and platinum, since platinum does not adhere well to the silicon dioxide surface itself.

Initial experiments were carried out in a multiple-target sputtering system equipped with a platinum target. However, since a titanium target was not available for this early work, the titanium was thermally evaporated in one vacuum system, and the substrates then removed and transferred to the sputtering system for the platinum deposition. This transfer of the substrates between deposition systems exposed the titanium layer to the room ambient, apparently causing oxidation and/or contamination to at least some extent of the titanium layers. Although the sputtered platinum had a good visual appear-

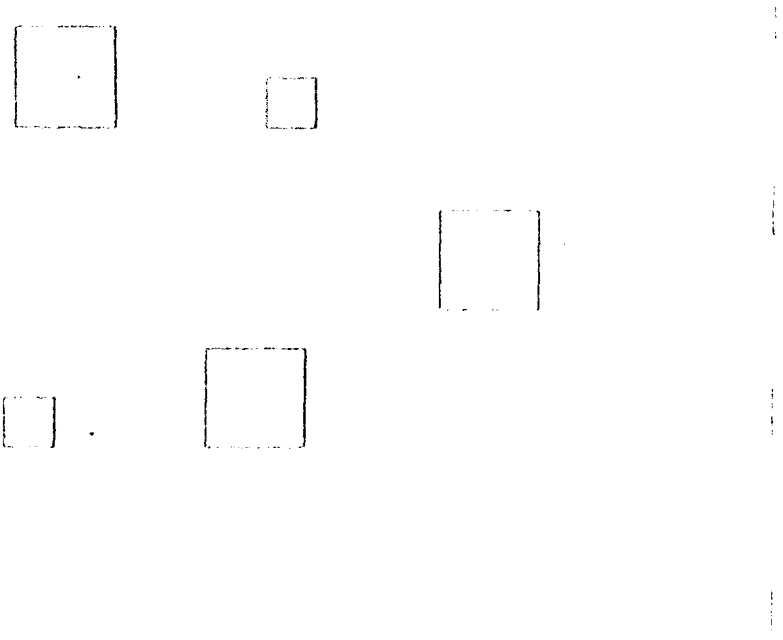


Figure 3. Etched 40 × 40 μm and 80 × 80 μm PZT islands.

ance on these substrates, subsequent heating of the substrates to temperatures greater than 550 °C in oxygen ambients, as would be required in the annealing of deposited ferroelectric films, caused the platinum to bubble and blister, leaving the surfaces unsuitable for the ferroelectric film deposition (fig. 4). This situation persisted until a suitable titanium target became available, and we could then sputter the titanium and platinum films sequentially without breaking vacuum.

After considerable experimentation to determine relative thicknesses for the glue and platinum layers, a good workable bottom electrode was obtained with a 300-Å glue layer followed by 2000 Å of platinum. These substrates could be heated to temperatures of 625 °C in oxygen for periods of 30 minutes without the physical appearance of the metal film being degraded. However, temperatures higher than 625 °C caused the platinum to form very fine pits and blisters, rendering it unsuitable for ferroelectric films requiring these higher temperatures. In our current efforts, we are trying to obtain more stable platinum films for the bottom electrode by adjusting the sputtering power and the relative thicknesses of the glue and platinum glue layers, and by being more meticulous in cleaning the silicon dioxide surface before sputtering.

For the top electrode, thermally evaporated and sputtered platinum films deposited through a shadow mask were used. Since these electrodes were directly on the PZT and because there was no high-temperature processing beyond this point, no adhesion problems

Figure 4. Blistered platinum layer.

were experienced between the platinum electrodes and the PZT, so that working ferroelectric capacitors were obtained.

The other technical area that received major attention in this initial effort was the defining of the top platinum electrode on the PZT. Because the number of PZT sample wafers was small, early experiments were conducted with platinum deposited on silicon dioxide test wafers. Two separate problems were encountered during these experiments. The first problem was to determine an acceptable procedure for imaging the photoresist on the silicon-dioxide/platinum surface. The second problem was to find an appropriate method for etching the platinum to form the top electrode.

The results of our first attempts to obtain good photoresist images on the platinum using a Kasper contact printer were unacceptable. Although a dyed photoresist that is designed for use on reflective metals was employed, the platinum caused such strong internal reflections within the photoresist that standing waves were produced, preventing the photoresist from exposing properly. As a result, when the photoresist was developed, the pattern was only partly and very unevenly developed. To solve this problem, we increased the exposure times for the photoresist from the standard 15 s to a full 30 s, and changed the developing time from 30 s to 1 minute. Finally, a 30-s, 300-W oxygen plasma descum cleaning was employed to remove any photoresist film that might remain on the surface. It is of particular importance to remove such films before wet etching operations, since a photoresist film even a few hundred angstroms thick can block the etch from attacking the desired surface. This procedure allowed us to obtain acceptable imaged patterns in the photoresist (fig. 5).

Wet etching of platinum is usually done in aqua regia at elevated temperatures. Since it was known that hot aqua regia strongly attacks photoresist, an alternative masking material needed to be used to define the patterns on platinum during the etching. Because silicon dioxide is highly resistant to aqua regia, it was decided to employ a chemical vapor-deposited silicon dioxide as the etch mask and to use the photoresist to pattern the silicon dioxide. However, because of severe undercutting, this method did not produce the well-defined geometries required. Subsequent experiments were conducted with an aqua-regia-like solution consisting of 1 part nitric acid, 7 parts hydrochloric acid, and 8 parts water, heated to 70°C for the etching. This etchant can be used with either the silicon dioxide etch mask or even photoresist by itself, and acceptably good results were obtained for platinum deposited on silicon dioxide (fig. 6). However, when this technique was employed to etch platinum on the PZT films, unacceptable results were obtained because the wet etch tended to attack the PZT, causing undercutting of the patterns (fig. 7).

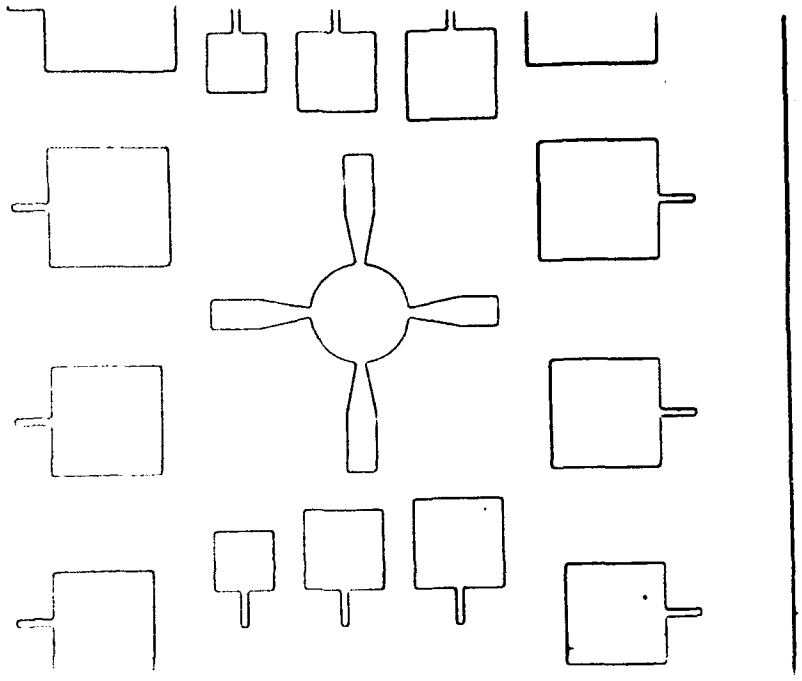


Figure 5. Imaged photoresist on platinum surface.

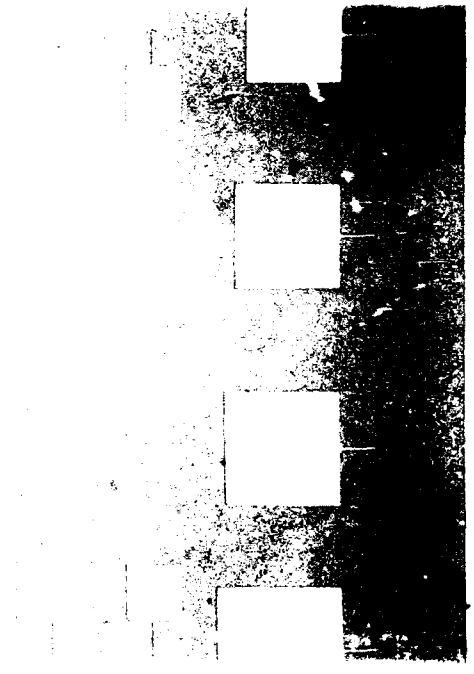
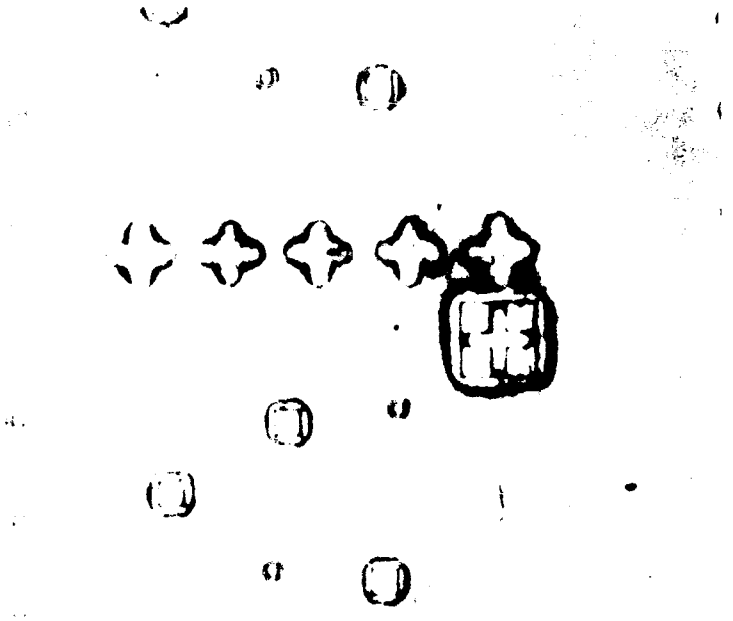


Figure 6. Wet etched platinum on silicon dioxide.

From these experiments, it became evident that wet etches that could be used with platinum on silicon dioxide were not compatible with platinum on PZT, and an alternative dry etching procedure was needed. One method that was available with the existing capabilities within the laboratory was to use the sputtering system in the etch

Figure 7. Wet etched platinum on PZT.



mode to sputter etch the platinum on the PZT. Before any actual etching was done, a number of runs were made to establish the relative sputtering etch rates of the platinum, PZT, and a number of possible masking materials. The etch rates at 125 W for all materials evaluated are shown in table 1. It can be observed that there is excellent etch rate selectivity between the platinum and the PZT. Also, a significant etch rate difference exists between the platinum and a number of other materials that could be used as etch masks to define the patterns. The most convenient masking material to use would be photoresist, since this can be easily applied and imaged to form the pattern. Although the photoresist has a relatively high sputtering rate, as shown in table 1, the standard applied thickness of about 1.2 µm appeared to be more than sufficient to mask the 2000 Å of platinum during the 4 to 5 minutes required to completely etch the platinum.

Table 1. Sputter etch rates for process materials

Material	Etch rate (Å/min.)
Photoresist	1200
Platinum	400
PZT	140
Silicon	420
Silicon dioxide	110
Silicon nitride	175

Test samples consisting of approximately 150 nm of sputtered platinum on PZT were coated with KTI 829 dyed photoresist spun on to a thickness of 1150 nm. The photoresist was exposed on the contact printer and developed using the previously determined procedure. The sputter etching was done at a power level of 125 W with the anode in its lowest position (approximately 5 cm from the shutter). Based on the etch rates obtained during the trial runs, a total etching time of 5 minutes was used. Following the etching, a profile of the photoresist pattern remaining was taken, as shown in figure 8. Although some of the step observed in the profile is due to PZT that may have been removed, it is clear that a sufficient amount of the resist has remained to protect the underlying platinum. The remaining photoresist was removed by plasma ashing. Figure 9 shows the platinum electrodes on the PZT layer.

Several more samples of platinum on PZT were sputter etched so that we could determine the uniformity of this process. At this time, the run-to-run variations in the etching rates appear to be too large for acceptable, consistent results on all samples. During one etching run, considerable arcing was noticed on the bottom sputter station electrode and on the sample itself. When the sample was removed from the sputtering system, most of the photoresist patterns and underlying platinum were observed to have been removed. Also, considerable residue, consisting of platinum specks and other loose material, was observed on the bottom sputtering station electrode. It is apparent that residue on the sputtering electrode can lead to electrical discharges between the top and bottom sputtering electrodes, and this can destroy the sample being etched. The arcing was not observed on the next sample run, after a thorough cleaning of the bottom sputtering station electrode. Further work is needed on the sputter etching technique for it to yield consistent results.

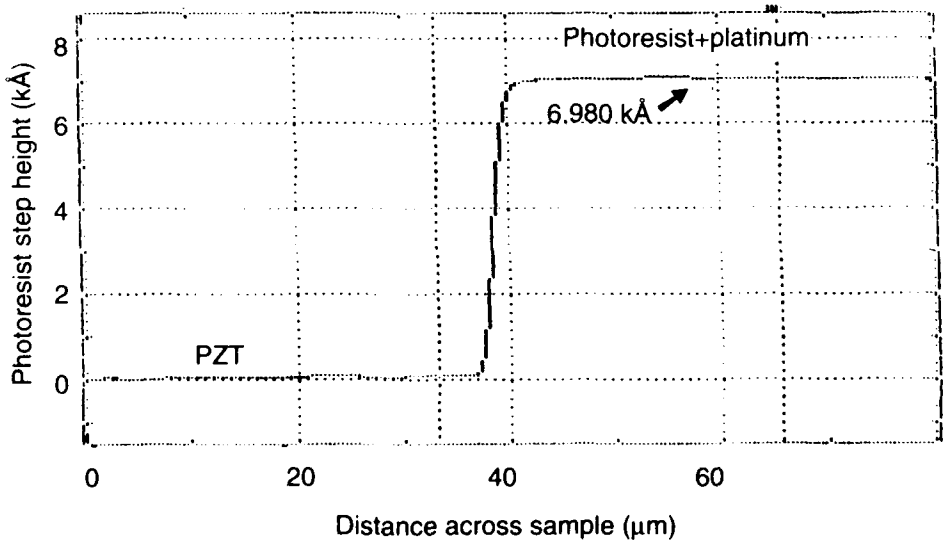


Figure 8. Photoresist/ platinum step after sputter etching.

Figure 9. Sputter-etched platinum electrode on PZT.

3. Conclusions

Considerable progress has been made to date in developing the techniques and procedures needed to fabricate the ferroelectric capacitor in a manner that is expected to be fully compatible with CMOS integrated circuit processing. Specifically, techniques have been developed to reliably etch the PZT films to form the capacitor body and to deposit the top platinum electrode. However, it is clear that problems remain relating to the bottom platinum electrode and the etching of the top platinum electrode that must be addressed before a full capacitor fabrication process can be considered to be established. In addition, the integration of the capacitor process with the CMOS circuitry remains to be addressed. Most important here is the question of interconnecting the ferroelectric capacitor with the underlying CMOS devices. A new mask set has recently been generated that will permit evaluating a number of integration issues.

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